UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,983	03/01/2004	Nathan Zommer	011775-010210US	1309

20350 7590 05/19/2005

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,983	ZOMMER ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 7-12 and 14 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Colwell et al.

In regards to claim 1, Colwell et al. inherently show a method for manufacturing a semiconductor power device in fig. 2b. It comprising: identifying an active region on a semiconductor die; identifying a first region (a region occupied by a first group of transistors [154]) in said active region; identifying a second region (a region occupied by a second group of transistors [171]) in said active region; identifying a third region (a region occupied by a third group of transistors [152]) in said active regions; providing a first cell design by which active cells in said first region will be fabricated; and providing a second cell design by which active cells in said second region will be fabricated; and providing a third cell design by which active cells in said third region will be fabricated, wherein first active cells (NMOS) fabricated according to said first cell design are different from second active cells (NMOS) fabricated according to said second cell design, wherein third active cells (PMOS) fabricated according to said third cell design are different from said first active cells and from said second active cells.

In regards to claim 2, Colwell et al. further disclose said first cell design and said second cell design include cell dimensions such that a cell density of said first region is different from that of said second region.

In regards to claim 3, Colwell et al. further disclose said first cell design includes at least one physical dimension different from that included in said second cell design.

In regards to claim 4, Colwell et al. inherently disclose said physical dimension includes a channel width because the gate width of first cell design is larger than that of the second cell design (col. 8, lines 42-48).

In regards to claim 5, Colwell et al. further disclose said physical dimension includes a cell die area (the first region is larger than the second region).

In regards to claim 7, Colwell et al. inherently disclose said first cell design differs from said second cell design with respect to current density because the transistors in the second region draw less current than that of the transistors in the first region).

In regards to claim 8, Colwell et al. inherently disclose said first cell design differs from said second cell design with respect to source resistance because the source regions in the second region are smaller than the source regions in the first region.

In regards to claim 9, Colwell et al. inherently disclose said first cell design differs from said second cell design with respect to transconductance because the current density of the transistors in the first region is different than that of the transistors in the second region.

In regards to claim 10, Colwell et al. inherently disclose said first cell design differs from said second cell design with respect to gain because the current density of the transistors in the first region is different than that of the transistors in the second region.

In regards to claim 11, Colwell et al. inherently disclose said first cell design differs from said second cell design with respect to threshold voltage because the transistors in

the second region have a smaller gate length than that of the transistors in the first region.

In regards to claim 12, Colwell et al. further disclose said first cell design and said second cell design are field effect transistors.

In regards to claim 14, Colwell et al. further disclose a semiconductor power device fabricated in accordance with the method of claim 1.

3. Claims 1 and 6 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kuroda et al.

In regards to claim 1, Kuroda et al. inherently shows a method for manufacturing a semiconductor power device in fig. 10A. It comprising: identifying an active region on a semiconductor die; identifying a first region (a region occupied by the NMOS transistors [103]) in said active region; identifying a second region (a region occupied by the PMOS transistors [102]) in said active region; identifying a third region (a region occupied by the bipolar transistors [101]) in said active regions; providing a first cell design by which active cells in said first region will be fabricated; and providing a second cell design by which active cells in said second region will be fabricated; and providing a third cell design by which active cells in said third region will be fabricated, wherein first active cells (NMOS) fabricated according to said first cell design are different from second active cells (PMOS) fabricated according to said second cell design, wherein third active cells (bipolar transistors) fabricated according to said third cell design are different from said first active cells and from said second active cells.

In regards to claim 6, Kuroda et al. further disclose said first cell design includes a material composition (n-type dopants in source and drain regions) for cells that is different from that of said second cell design (p-type dopants in source and drain regions).

4. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: The major difference in the claims not found in the prior art of record is the first cell design and the second cell design are memory cells.

6. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
May 14, 2005

Steven Loke
Primary Examiner